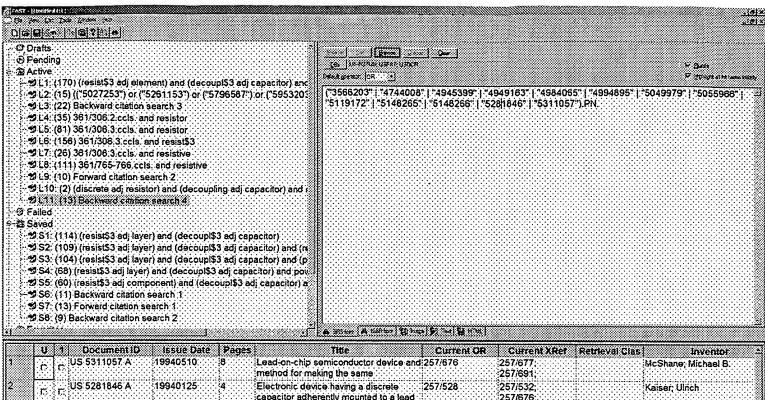
Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	823	"174"/\$.ccls. and (resist\$3 adj layer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/21 16:14
L2	149	"174"/\$.ccls. and (resist\$3 adj layer) and power and ground	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/21 16:25
L3	188	"361"/\$:ccls: and (resist\$3 adj layer) and power and ground	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/21 16:37
L4	15	("4777718").URPN.	USPAT	OR	ON	2005/02/21 16:51



	U		Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Clas Inventor
1	c	С	US 5311057 A	19940510		Lead-on-chip semiconductor device and method for making the same	257/676	257/677; 257/691;	McShane; Michael B.
2	г	г	US 5281846 A	19940125		Electronic device having a discrete capacitor adherently mounted to a lead	257/528	257/532; 257/676;	Kaiser, Ulrich
3			US 5148266 A	19920915		Semiconductor chip assemblies having interposer and flexible lead	257/773	257/668 257/669	Khandros; Igor Y. et el.
4	r		US 5148265 A	19920915	(Br. e. e. e. e. e. e.	Semiconductor chip assemblies with fan-in leads	257/773	257/668; 257/669;	Khandros; Igor Y. et al.
5	Γ	F	US 5119172 A	19920602		Microelectronic device package employing capacitively coupled	257/684	257/659; 257/E23.144	Cho; Frederick Y, et al.
8	r	C	US 5055966 A	19911008		Via capacitors within multi-layer, 3 dimensional structures/substrates	361/321.3	174/52 4: 257/774;	Smith; Hal D. et al.
7	r	r	US 5049979 A	19910917		Combined flat capacitor and tab integrated circuit chip and method	257/723	257/784; 257/916;	Hashemi, Seyed H. et al.
8	т	г	US 4994895 A	19910219		Hybrid integrated circuit package structure	257/791	257/874; 257/684;	Matsuzaki; Toshio et al.
e Vints							j		<u>.t</u>